Investigating Nanoscale Joule Heating in Lithium Niobate Memristors

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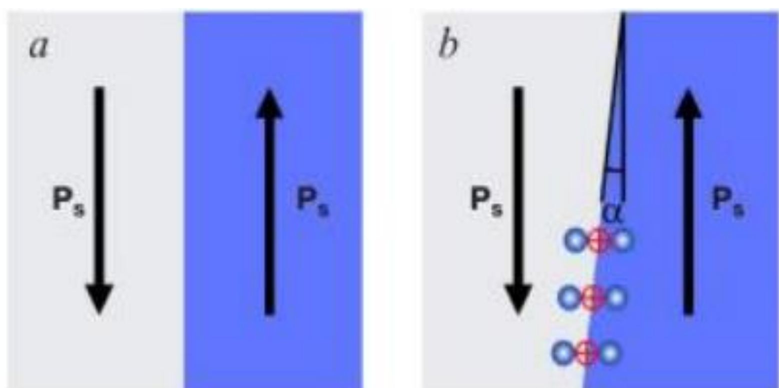
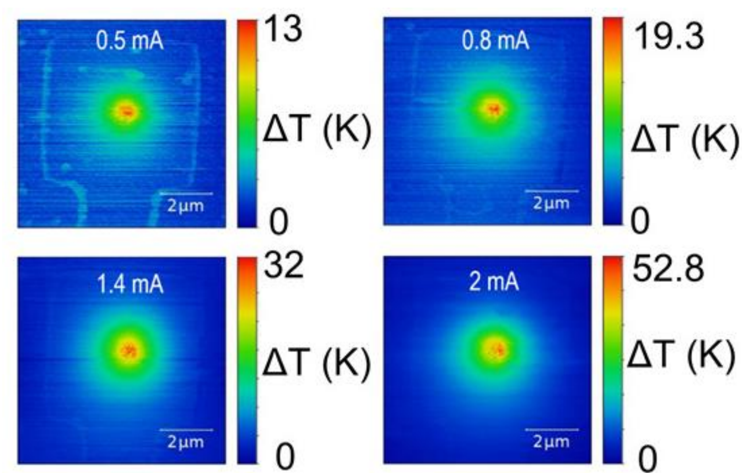
CONCEPT & BACKGROUND

Domain walls in ferroelectrics are interfaces that separate polar domain variants. They can be created, erased or moved by applied voltages, and in this sense are reconfigurable. Certain domain wall types can also have higher electrical conductivity than the bulk material.

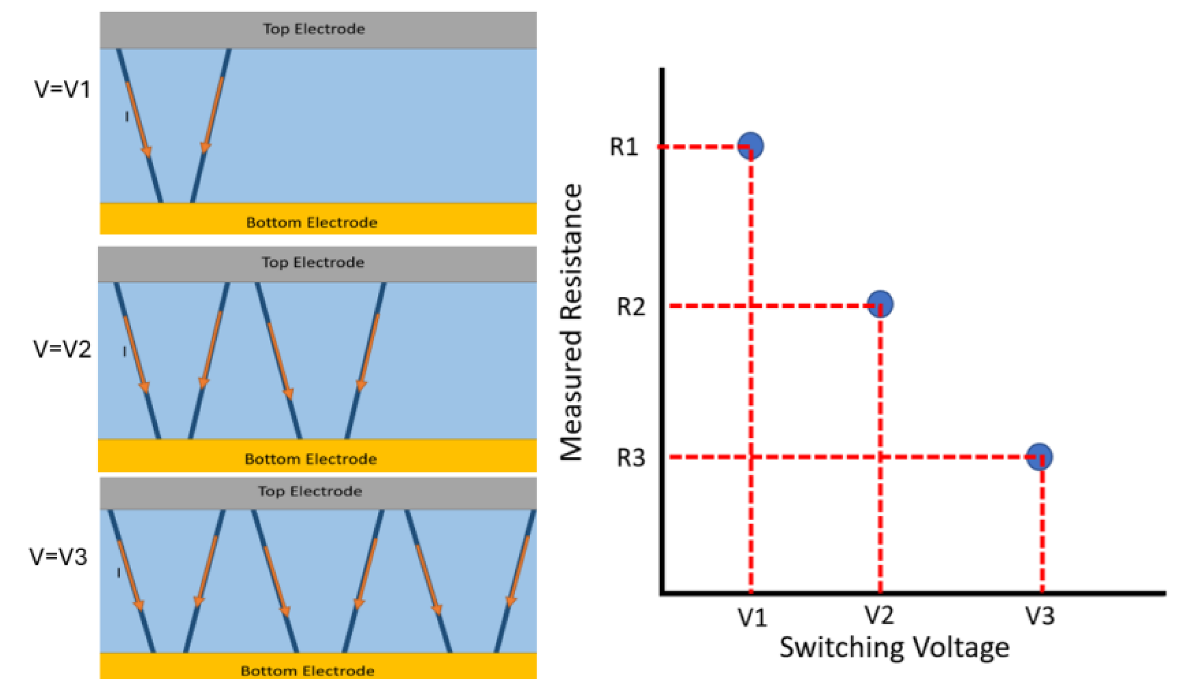


Schematic of domains (regions of polarisation) and the boundary between them (domain walls) and how this leads to conductive domain walls. [1]

The number of domain walls connecting device electrodes determines the current, and hence device resistance (right). Multiple non-volatile resistance levels can be voltage programmed to create a multistate memory device i.e. a **memristor.** [2,3]



Thermal mapping of conductive filaments in memristor devices experience joule heating [4]

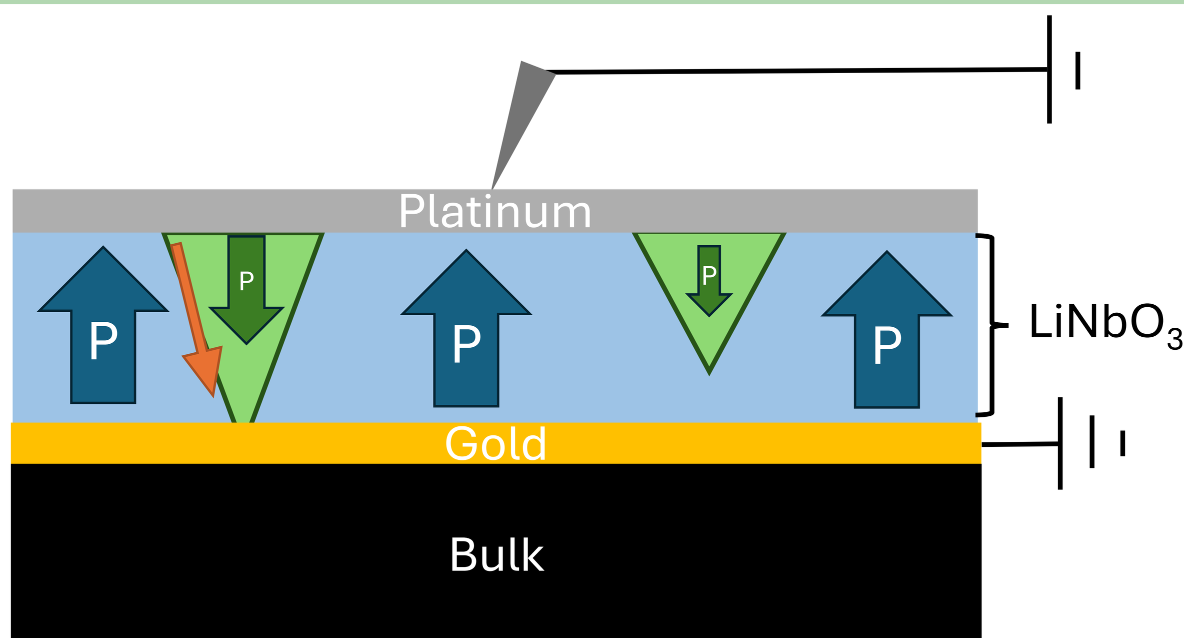


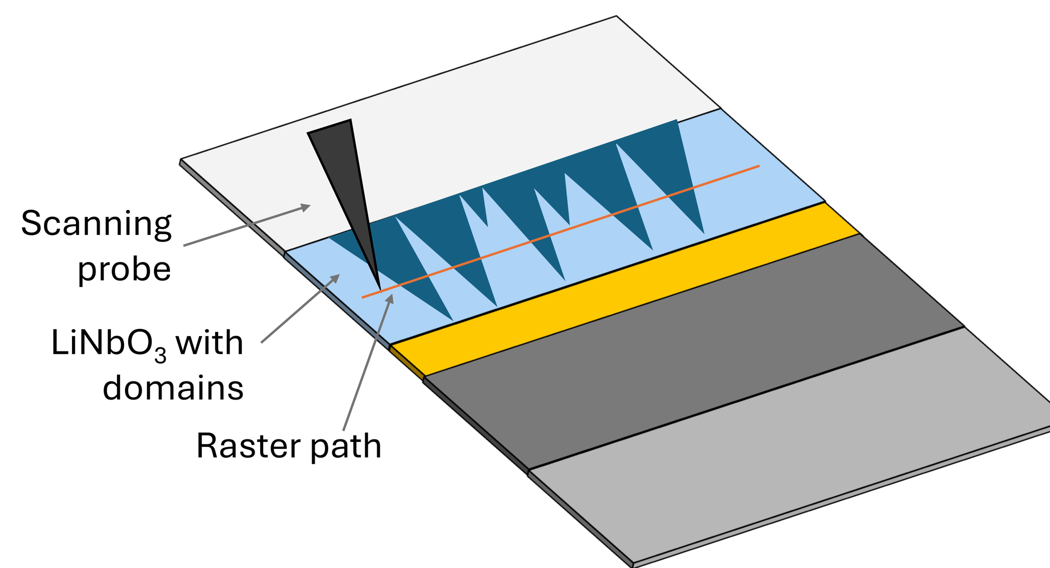
Schematic of varying number of conducting domain walls and associated device resistance.

These conductive domain walls experience localised Joule heating when biased. Unregulated self-heating in filament conductor based resistive memory devices (left) can affect performance and efficiency. Nanoscale temperature mapping is required for better understanding of these heating processes and to enable improved device efficiency.

METHODS

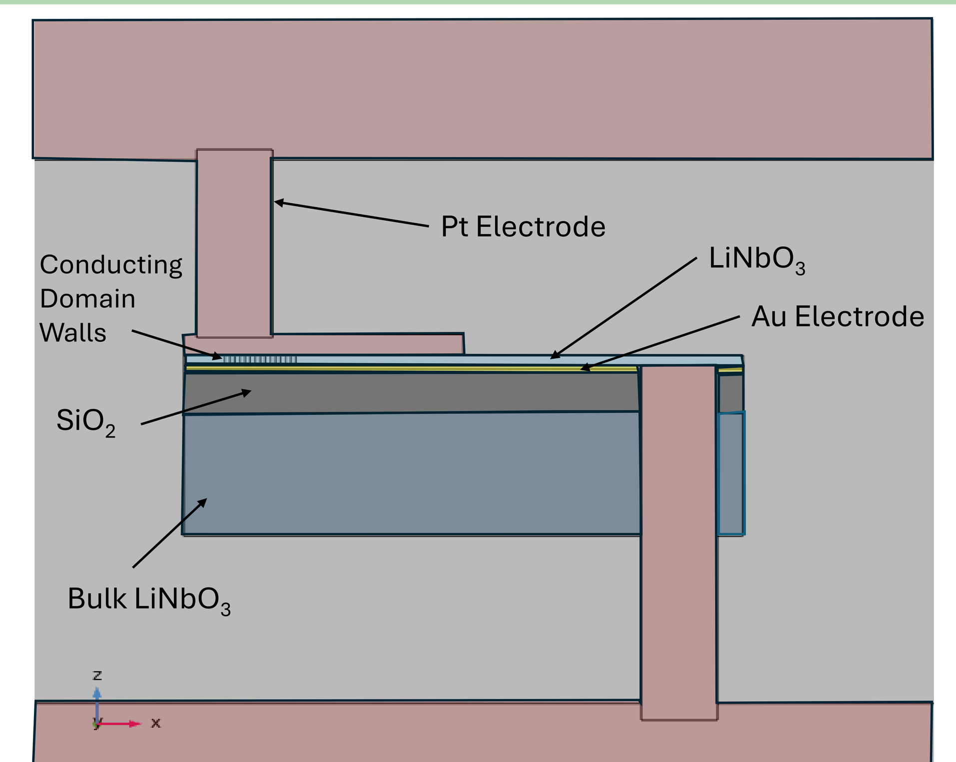
Domain walls were introduced to thin-film ferroelectric $LiNbO_3$ by voltage poling (below). The size of the domains increases with increased applied voltage; conductive paths are formed when the domain walls connect top and bottom electrodes.



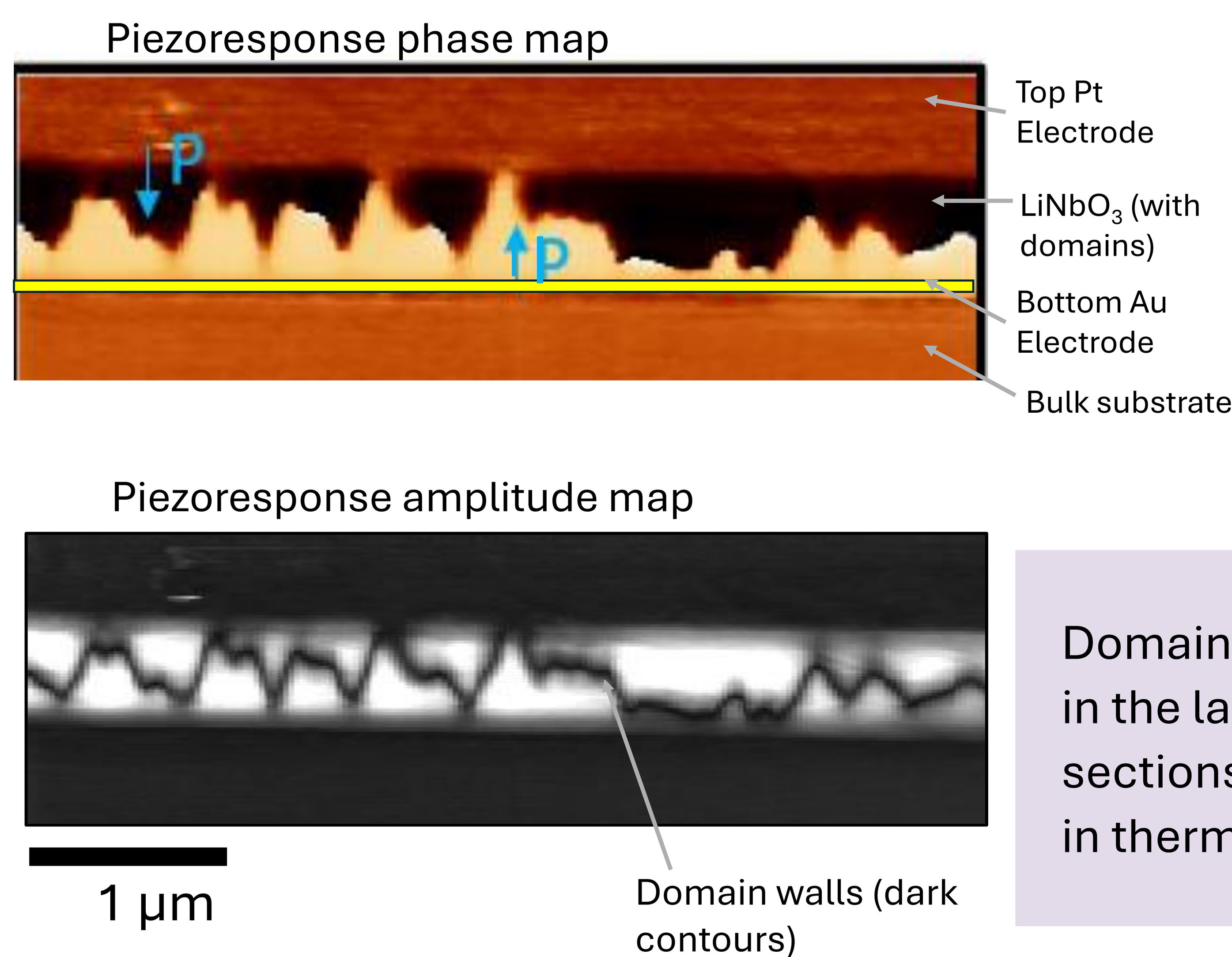


The presence of domain walls within the real device was confirmed using Piezoresponse Force Microscopy (PFM) imaging of the device cross section (fabricated by Focused Ion Beam machining and schematised above). For thermal imaging, the active region can be contacted directly by the scanning probe while bias is supplied through planar surface electrodes.

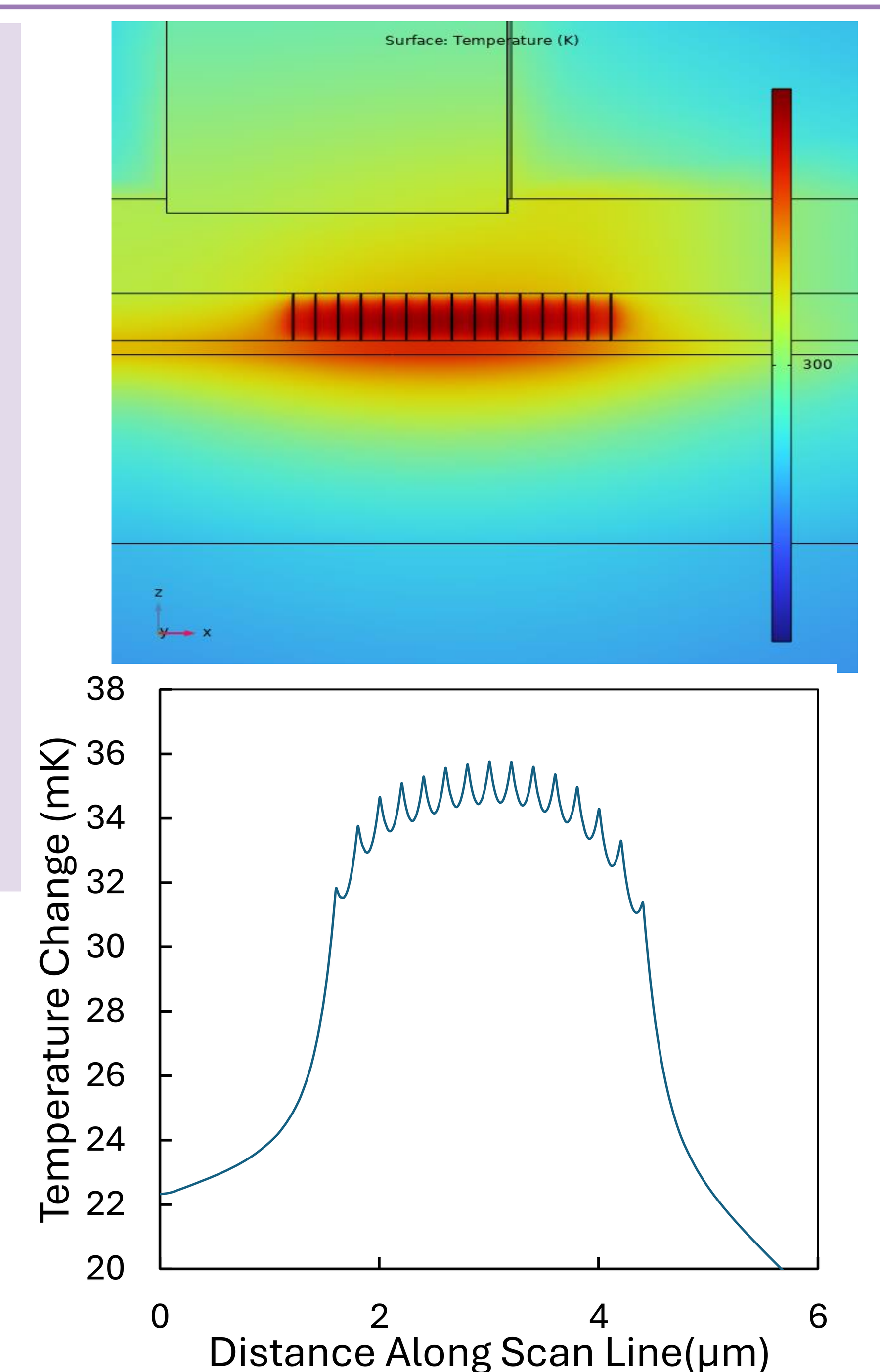
The experiment was also simulated using COMSOL finite element modelling. The memristor device was recreated and the temperature of the current-carrying domain walls was calculated when the device was powered.



RESULTS



Finite element modelling estimates temperature changes of ΔT~30mK for a 10µA current flowing through the device cross-section, when placed on SiO_2 substrate. An increased ΔT of ~70 mK is observed for 10 µA current in the absence of the substrate. Direct imaging of the heated filaments therefore comes at the cost of reduced temperatures compared to the buried devices (ΔT of ~10 K), due to the effects of small active volume in the cross section (~10 x 0.5 x 0.3 µm^3) and substrate heat sinking



Domains and domain walls were preserved in the lamella (left). Electroded device cross sections were successfully fabricated to use in thermal imaging investigations.

REFERENCES

[1] Kislyuk, Aleksandr M., et al. Modern Electronic Materials 9.4 (2023): 145-161.
[2] McConville, James PV, et al. Advanced Functional Materials 30.28 (2020): 2000109.
[3] Seidel, Jan, et al. Nature materials 8.3 (2009): 229-234.
[4] Nandi, Elliman et. al. *ACS Applied Materials & Interfaces.* 14,25 (2022)